Measurement-Based Closed-Form Modeling of Surface-Mounted RF Components

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***Abstract*—An understanding of the parasitic and packaging effects of passive surface-mounted devices (SMDs), including characterization of the pertinent interconnects, is required for developing robust equivalent-circuit models that are useful in RF and microwave computer-aided design. In this paper, we develop a procedure for modeling SMD inductors and capacitors, which incorporates the nonideal behavior associated with frequency dispersion, board layout, component parasitics, and device packaging. The equivalent-circuit parameters are extracted in closed-form from accurate *in-situ* measurement of the component's S-parameters, without the necessity for cumbersome optimization procedures normally followed in RF equivalent-circuit synthesis.**

***Index Terms*—CPW, equivalent-circuit modeling, measurement-based modeling, microwave CAD, network analyzer, package and layout parasitic effects, RF component measurements, S-parameters.**

I. Introduction

PASSIVE surface-mounted devices (SMDs), such as thin-film inductors, capacitors, and resistors are extensively employed in the RF industry. These components are wave soldered or wire bonded onto associated pads on a printed circuit board (PCB). At radio frequencies, the combination of component packaging, pad footprint, PCB layout, and the substrate interaction causes detrimental local parasitic effects such as resonant coupling, crosstalk, signal loss, signal distortion, etc. Circuit modeling of these devices should, therefore, consider the environment in which the devices will be operated—a process henceforth termed as *extrinsic modeling*. This should be contrasted with the *intrinsic* measurement-based *modeling*, in which the component is measured *by itself* on an impedance analyzer, for example, without regard to the application environment. Thus, extrinsic RF circuit models account for the *external* device parasitic effects associated with the pad layout, dielectric substrate, interconnect structure, etc., *in addition* to the inherent physical characteristics of the device itself. In contrast, the conventional intrinsic circuit models consider only the latter. By definition, any device model should account for the inherent physical characteristics of the device. The extrinsic model adds the parasitic influence of the component's external functional environment to the intrinsic model and, thus, *provides a realistic basis in design applications*.

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Synthesis of equivalent-circuit models for discrete components usually involves either electromagnetic (EM) simulations or measurements, followed by curve fitting the resulting data to the response of a desired model, chosen on the basis of designer's *a priori* knowledge of the component [1]–[5]. The curve-fitting process entails complex optimization routines and, thus, becomes unmanageable, except for simple circuit configurations. There are two main disadvantages in using global optimization to develop equivalent-circuit models. First, it is impractical in such an optimizer to accurately evaluate the frequency dependence (dispersion, loss, etc.) of the model since the process yields frequency-independent ideal elements. Second, the complex physical attributes found in today's circuits, such as microelectromechanical system (MEMS) packaging and novel materials assemblies, demand co-simulation between EM simulators, circuit simulators, and optimizers. This requires considerable computer resources and, even then, it becomes difficult to ensure that the optimization indeed converged to the correct solution. To circumvent this optimization process, some authors have attempted to synthesize equivalent circuits in closed form, valid at either low frequencies or over a narrow frequency range, where coupling, package, and loss mechanisms are not predominant (e.g., [6]–[10]). These closed-form expressions also yield constant element values, albeit valid over a narrow-frequency band. In order to span a wide-frequency band, one sweeps over several adjacent bands and adjusts the equivalent-circuit parameters for each band. In computer-aided design (CAD) applications, the utility of such a problem-dependent approach is very limited. In summary, the usually frequency-dependent layout- and package-specific parasitic effects, pertinent to the design of broad-band amplifiers and other high-speed circuits, are not considered in the equivalent-circuit representation provided by frequency-selective CAD models.

In this paper, we develop a procedure for deriving comprehensive frequency-dependent equivalent-circuit models of SMD inductors and capacitors, starting from broad-band S-parameter measurements of the device on a network analyzer (NA). The component is measured in a grounded coplanar waveguide (CPWG) fixture representing the circuit environment of the application. The impedance mismatch between the fixture and NA is error-corrected by direct calibration at a reference plane located at the edge of the component footprint (see Fig. 1), using short, open, load, and thru (SOLT) calibration standards, developed specifically for the coplanar waveguide (CPW) environment [7], [11]–[13]. Thus, the resulting circuit model exclusively captures the sought-after parasitic interaction between the PCB environment and component. Such models can potentially

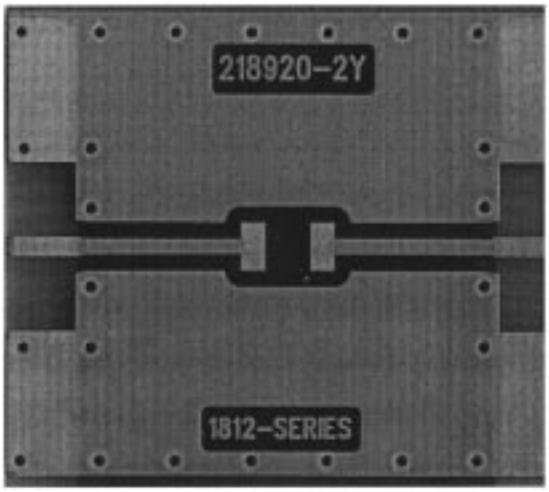


Fig. 1. CPW pad and trace configuration for an SMD component. The pad edges on the feed lines define the reference planes.

reduce the number of design iterations in a practical situation since the model is based on accurate *in-situ* measurements tied to the application environment. Besides, as will be discussed later in this paper, these extrinsic models also improve the accuracy of circuit simulations. The CPW interconnects needed in a physical layout are characterized for their attenuation constant, phase constant, and characteristic impedance using either full-wave EM simulations or measurement on test coupons (transmission lines) of different lengths.

This paper is organized as follows. In Section II, we first summarize the importance of synthesizing an extrinsic circuit model from measured component data, and then present the derivation of such models for SMD inductors and capacitors. We then outline the calibration and measurement technique in Section III, following the procedure presented in [7]. We also include results to verify accuracy of the calibration. Section IV contains measured and modeled data for SMD inductors, capacitors, and surface-mounted ferrite chokes. The data pertinent to characterization of CPW interconnects, and a circuit implementation, involving measurement validation on a low-pass filter designed using the extrinsic component models, are also presented in Section IV. Section V summarizes the conclusions of the study.

II. Equivalent-Circuit Extraction

A. Extrinsic Versus Intrinsic Modeling

Component models supplied by the manufacturer, or those derived from measurements on inductance, capacitance, resistance (LCR) meters, bridges, and impedance analyzers [14] describe the intrinsic characteristics of the component and, therefore, preclude package and layout parasitics associated with the motherboard and circuit housing. As defined in Section I, an *intrinsic* circuit model does not include these parasitic effects, whereas an *extrinsic* model does. Intrinsic specifications are of limited value in design. Besides being inaccurate, designing a circuit based on the nominal value provided by the intrinsic model inevitably leads to considerable tuning and testing after board fabrication.

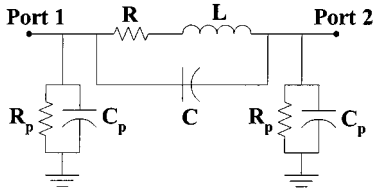


Fig. 2. Two-port extrinsic equivalent-circuit model for inductor.

The measurements for the derivation of extrinsic circuit models of SMD components employ the CPWG layout shown in Fig. 1. The board is mounted in a coaxial metal fixture, which connects to the NA through precision coaxial cables. The appropriate measurement fixture and CPWG calibration standards are discussed in Section III. After calibration, the reference plane is established at the outside edges of the two component pads shown in Fig. 1. In other words, the layout interface between the device and its footprint are included in the measurement, whereas the connecting lines and the coaxial transitions at the fixture ends are calibrated out. Of course, one must exercise caution in any on-board calibration and should attempt to minimize the return-loss variations across the transitions by proper fixture design. With an SMD inductor inserted between the pads, the board parasitics may significantly change the inductor circuit model derived from intrinsic measurements. The manner in which the layout parasitics influence the component's intrinsic model depends on the frequency and contact between the SMD and pad (solder bump resistance, wire-bond inductance, etc.). Therefore, a design based on the intrinsic equivalent circuit can become quite off-centered when the components are mounted on a board, and meeting the design specifications may require considerable bench testing. For example, the parasitic effects caused by a different layout may result in different measured resonant frequencies and Q factors for the *same* inductor.

An example of the extrinsic circuit model of an SMD inductor is shown in Fig. 2. The series resistance R includes the SMD package losses, skin, and proximity resistive effects of the winding, as well as the pad or trace losses. Likewise, the series capacitance C represents the self-capacitance of the inductor package and the capacitance between the pads. The pad is simply a step-in-width inductive transition [15], [16] and augments the series inductance of the intrinsic model. The total inductance is denoted as L. The dielectric losses in the substrate introduce a shunt conductance $G_p = 1/R_p$, and the capacitance to ground of each pad introduces a shunt C_p, which is also influenced by the substrate. It is evident that the resonant frequency and Q of the intrinsic *RLC* model are altered by parasitic loading. We assume that the operating wavelength is large enough for the parasitics to be considered local to the SMD component. Thus, distributed parasitic effects, which may become prominent at higher frequencies, are not considered in the proposed modeling approach. Furthermore, in practical applications, since we use SMD inductors and capacitors below their first resonance, we do not consider the higher order resonant effects in the equivalent-circuit representation.

To summarize, if we base the circuit design on the extrinsic circuit model, the increased accuracy attained by incorporating

board parasitics can potentially reduce the number of design cycles. Furthermore, using an accurate library base of extrinsic equivalent-circuit models, it is feasible to accomplish most of the design centering on a circuit simulator instead of the bench.

B. Closed-Form Inductor Model

The direct RF measurement of the model parameters L, R, and C of a surface-mounted inductor is difficult because of their strong interaction with the board parasitics. Typically, any of these parameters can be obtained indirectly from measurable parameters such as impedance, quality factor, and resonant frequency. As alluded earlier, we measure the S-parameters of an SMD inductor in a CPWG fixture using a vector NA, with on-board calibration performed at the reference planes shown in Fig. 1. We now describe how one can synthesize the equivalent circuit, shown in Fig. 2, from these measurements. The synthesis is accomplished in closed form without the cumbersome numerical procedures (e.g., optimization) usually involved in obtaining physical device parameters from RF measurements.

Denoting the series impedance in Fig. 2 as Z and the shunt admittance as Y_p, we have

$$Z = \frac{R + j\omega L}{1 - \omega^2 LC + j\omega RC} \tag{1}$$

$$Y_p = G_p + j\omega C_p. \tag{2}$$

The measured S-parameters are first transformed into the admittance parameters using [15]

$$Y_{11} = Y_c \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{\Delta_S} \tag{3}$$

$$Y_{12} = -Y_c \frac{2S_{12}}{\Delta_S} \tag{4}$$

$$Y_{21} = -Y_c \frac{2S_{21}}{\Delta_S} \tag{5}$$

$$Y_{22} = Y_c \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{\Delta_S} \tag{6}$$

where $Y_c = 1/Z_c$ is the characteristic port admittance, and $\Delta_S = (1 + S_{11})(1 + S_{22}) - S_{12}S_{21}$. Due to reciprocity, we have $S_{12} = S_{21}$ and, hence, $Y_{12} = Y_{21}$. The block immitances of the π-equivalent circuit in Fig. 2 follow from the Y-parameters as

$$Z = -\frac{1}{Y_{12}} \tag{7}$$

$$Y_1 = Y_{11} + Y_{12}$$

$$Y_2 = Y_{22} + Y_{12}. \tag{8}$$

Due to symmetry, we can equate the shunt admittances at either port in Fig. 3 as $Y_1 = Y_2 = Y_p$, with Y_p represented in terms of the desired circuit model using (2). The model for the series impedance Z is given in (1). Thus, the admittance parameters in (7) and (8) are known at each measured frequency, and the objective is to compute the equivalent-circuit elements in Fig. 2 *as functions of frequency* using (1) and (2). From (2), we calculate the shunt conductance and capacitance as

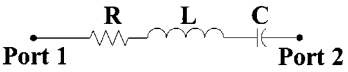


Fig. 3. Two-port extrinsic equivalent-circuit model for a capacitor without the shunt parasitics.

$$G_p = \mathrm{Re}(Y_p) \tag{9}$$

$$C_p = \frac{\mathrm{Im}(Y_p)}{2\pi f}. \tag{10}$$

The series impedance $Z(\omega)$ in (1) presents two (real) equations to determine the three variables L, R, and C. We shall show next that one of the three variables can be computed from the resonant characteristics; thus, leaving two degrees of freedom to be addressed by the two independent equations in (1). $Z(\omega)$ resonates at the frequency ω_0 with a quality factor Q, both of which can be obtained explicitly from the measured data. The resonant frequency is determined as the frequency at which $\mathrm{Im}(Z) = 0$, and Q is computed from the observed 3-dB bandwidth $\Delta\omega$ of the impedance magnitude as $Q = \omega_0/\Delta\omega$. Using circuit theory, the resonant frequency and quality factor for $Z(\omega)$ may also be calculated from Fig. 2 as

$$\omega_0 = \frac{1}{\sqrt{L_0 C}} \left(\frac{Q^2}{1 + Q^2}\right)^{1/2} \tag{11}$$

$$Q = \frac{\omega_0 L_0}{R_0} \tag{12}$$

where L_0 and R_0 denote inductance and resistance, respectively, at the resonant frequency. The impedance $Z(\omega) = Z_r(\omega) + jZ_i(\omega)$ in (1) may then be written as

$$Z(\omega) = \frac{R + j\omega L^2 C(\omega_0^2 - \omega^2)}{(1 - \omega^2 LC)^2 + (\omega RC)^2}. \tag{13}$$

At the resonant frequency, let $Z_0 \equiv Z(\omega_0)$ (a real number) be the impedance. Using (11) and (12) in (13), with $\omega = \omega_0$ substituted, we obtain

$$R_0 = \frac{Z_0}{1 + Q^2} \tag{14}$$

$$L_0 = \frac{QR_0}{\omega_0}. \tag{15}$$

Due to the miniature windings, the self-capacitance of SMD inductors is practically independent of frequency, and follows from (11) as

$$C = \frac{1}{\omega_0^2 L_0} \frac{Q^2}{1 + Q^2}. \tag{16}$$

It is assumed that the small inter-pad capacitance contributes negligibly to the inductor's self-resonance. Therefore, knowledge of the resonant frequency, quality factor, and impedance at resonance facilitates unique determination of one of the three

circuit variables for the SMD inductor, namely, the series capacitance C. After some algebra, the remaining two variables, the *frequency-dependent* inductance and resistance, can be obtained in closed form (see the Appendix) as follows:

$$\omega L(\omega) = \frac{Z_i(\omega) + \omega C|Z(\omega)|^2}{\left[1+\omega C Z_i(\omega)\right]^2 + \left[\omega C Z_r(\omega)\right]^2} \tag{17}$$

$$R(\omega) = \frac{Z_r(\omega)}{\left[1+\omega C Z_i(\omega)\right]^2 + \left[\omega C Z_r(\omega)\right]^2}. \tag{18}$$

These expressions are adequate for modeling SMD inductors at frequencies below the second resonance. At these frequencies, the distributed effects of the equivalent-circuit model can be neglected. Besides modeling SMD inductors, (17) may also be used to compute the incremental increase in inductance of a ferrite choke at radio frequencies over that of a commensurate air coil. Thus, the effective permeability can be computed for wide-band ferrite chokes utilized to suppress electromagnetic interference (EMI) in PCBs [17].

C. Closed-Form Capacitor Model

The equivalent-circuit representation for the SMD capacitor follows the same procedure as defined for the inductor. The measured S-parameters are first transformed into the admittance parameters using (3)–(6), and the series impedance and shunt admittance of the π-equivalent circuit are computed from (7) and (8). For the capacitor, the equivalent circuit consists of a series connection of R, L, and C, as shown in Fig. 3. By duality from the inductor model, we assume that the stray inductance L is invariant with frequency, thus leaving two degrees of freedom, i.e., $R(\omega)$ and $C(\omega)$, to be determined from the impedance in (7).

The series resonant circuit has minimum impedance at resonance, which is not as sharp as the peak resonance in the admittance curve. Therefore, it will be more accurate to calculate the resonant characteristics from the inverse of $Z(\omega)$ defined in (7) (or the equivalent admittance). The quality factor is still given by (12), but the resonant frequency is calculated using

$$\omega_0 = \frac{1}{\sqrt{L_0 C_0}}. \tag{19}$$

Both Q and ω_0 are computed from the peak of the admittance curve. The impedance in Fig. 3 is given by

$$\begin{aligned} Z(\omega) &= Z_r(\omega) + jZ_i(\omega) \\ &= R(\omega) + jQ\frac{\omega R_0}{\omega_0}\left(1 - \left(\frac{\omega_0}{\omega}\right)^2 \frac{C_0}{C(\omega)}\right). \end{aligned} \tag{20}$$

At resonance, $R_0 \equiv R(\omega_0) = Z_r(\omega_0)$ is computed from the measured data, $L = L_0$ is determined from (15), and using (19), the capacitance $C_0 \equiv C(\omega_0)$ is given by

$$C_0 = \frac{1}{\omega_0^2 L_0}. \tag{21}$$

At frequencies off the resonance, it follows from (20) that (see the Appendix)

$$R(\omega) = Z_r(\omega) \tag{22}$$

$$C(\omega) = \frac{1}{\omega\left(\omega L_0 - Z_i(\omega)\right)}. \tag{23}$$

D. Series Versus Shunt Connection

The analysis presented in Sections II-B and II-C is valid when the SMD element is connected in series with the incoming and outgoing transmission lines (see Fig. 1). This analysis is also applicable to a shunt connection if the shunt path involves a transmission line to ground. However, in practical circuits, when many components are involved, ground connection via a transmission line consumes considerable real estate on the printed substrate, and is thus undesirable. Furthermore, because of the dimensions of practical CPW transmission lines necessary to achieve 50- or 75-Ω characteristic impedance, the spacing between the signal line and adjacent ground trace becomes too small to allow any space for pads. Therefore, in the circuits realized in this research, we have connected a shunt element directly between the signal trace and ground without using any pads. The equivalent-circuit model for the shunt element is thus obtained from the previous analysis of series elements, precluding the pad parasitic effects or the shunt path of the π-equivalent circuit in Fig. 2.

III. Calibration and Measurement

The measurements are made on an FR-4 board mounted in a metal fixture with return loss better than -30 dB and insertion loss lower than 0.4 dB over a 1-MHz–3-GHz band. This fixture interfaces with precision coaxial connectors and cables on the vector NA. In order to replicate the environment of the application (CATV RF distribution amplifiers), a 75-Ω CPWG transmission medium has been chosen for the PCB. The trace layout for the measurement, including the component pads, is shown in Fig. 1. Several vias are stitched on either side of the center conductor to provide continuity between lateral and bottom ground planes. The intended reference plane for the measurement of the S-parameters is at the junction between the coplanar trace and pad on either side (see Fig. 1). Error correction of the measured S-parameters involves calibration of the cable effects, connector and other transition mismatches, transmission-line loss, and dispersion up to this reference plane. We have designed four precision standards (i.e., SOLT) on the same board as the measurement trace (see Fig. 4) for a 12-term error correction at the reference planes [7], [11]. These calibration standards depend on the package size, as illustrated in Fig. 4, with the IEC 1812 pad dimensions. These standards replace the NA's coaxial calibration standards, which place the reference plane at the center conductor edges of the coaxial connectors on the fixture, but not at the edges of the component pads depicted in Fig. 1. The SOLT calibration procedure involves defining the standards precisely to the NA in terms of what are known as *calibration constants* [12], and performing a user calibration.

The *short*, *load* and *thru* are of zero length offset and 75-Ω impedance. The *short* is constructed by joining the center conductor and the lateral ground at the reference plane location (Fig. 4). Additional vias are stitched around this connection. For better impedance matching, the transition from the center conductor of the coaxial interface to the CPW signal trace is

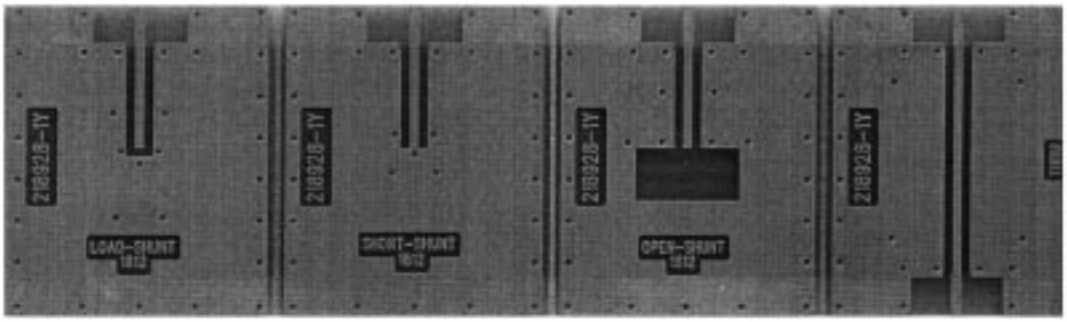


Fig. 4. On-board CPW calibration standards. (a) Load. (b) Short. (c) Open. (d) Thru.

made through a low-loss microstrip line. All the exposed copper is gold plated on signal traces and ground planes. A precision lumped chip resistor of 75 Ω is connected at the reference plane for the *load* standard (actually, to reduce the inductance of the resistor package, two 150-Ω resistors are connected in parallel). To minimize the influence of any package-specific parasitic effects of the resistor, small-footprint (IEC 0603) resistors are employed. It is assumed that the load reflection coefficient remains constant with frequency over the intended bandwidth of 1 MHz–3 GHz so that a precision lumped-element load can be justified. The accuracy of calibration using this load will be verified by independent measurements later in this section. Since the CPW *thru* standard has zero offset, its length is exactly equal to twice the distance between the end of the microstrip connector and the on-board measurement reference plane (see Fig. 1). Due to the zero offset of these three standards, short, load, and thru, we need not specify any calibration constants for these, other than the 75-Ω line impedance. An ideal open circuit is impossible. The nonideal *open* (Fig. 4) presents fringe capacitance at the end, which needs to be described as a function of frequency to the NA. This capacitance is measured independently using the procedure described in [7], and the frequency dependence is incorporated by fitting a third-order polynomial to the measured data. The polynomial coefficients are input to the NA as calibration constants for the board *open* standard. All the calibration constants for the four standards in Fig. 4 are recorded and stored in the NA's internal memory, where they are recalled before each calibration. By calibrating with these standards instead of the coaxial accessories supplied with the NA, we enable the NA to perform error-corrected measurements on SMD components at the *on-board* reference planes depicted in Fig. 1 instead of the standard coaxial interfaces. It should be noted that these SOLT standards are designed as *in-house* alternatives to on-board calibration in an environment not conducive to using commercial on-wafer probes. In our application, the frequency range and characteristic impedance made the CPW line pitch much larger than typically used in microwave circuits, and no commercial probes were available. Next, we present some results pertaining to accuracy of the calibration standards depicted in Fig. 4.

Fig. 5 displays the insertion loss of the uncalibrated fixture, measured between the coaxial reference planes with a 3.8-cm-long CPW transmission line mounted in the fixture. The insertion loss is better than 0.4 dB over the 3-GHz bandwidth of interest. Since reference planes are established at

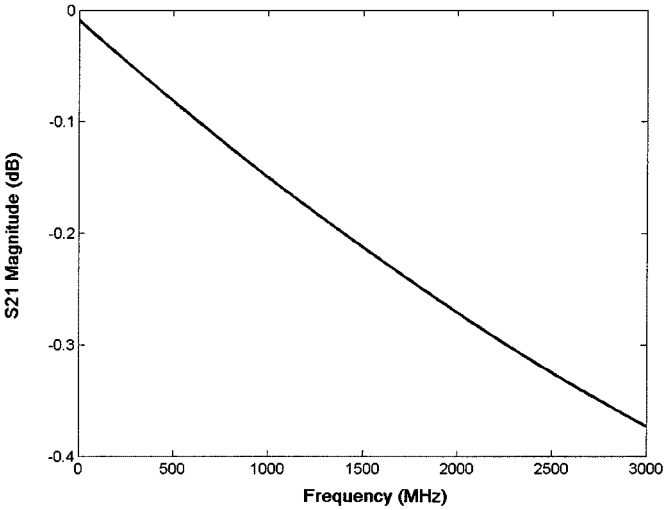


Fig. 5. Insertion loss of a CPW transmission line, measured in an *uncalibrated* fixture.

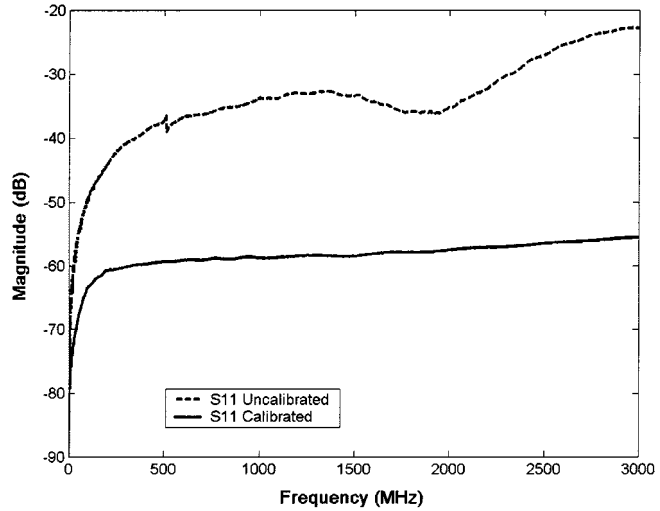


Fig. 6. Improvement in return loss of the *load* standard after calibration.

the component pad edges in Fig. 1 using a zero-length *thru* calibration standard, this insertion loss is corrected in actual SMD measurements. Fig. 6 depicts the return loss of the *load* calibration standard, measured in the same fixture, before and after calibration. The uncalibrated fixture yields a return loss better than 30 dB up to 2.5 GHz. After calibration, the maximum return loss measured is about −57 dB at 3 GHz,

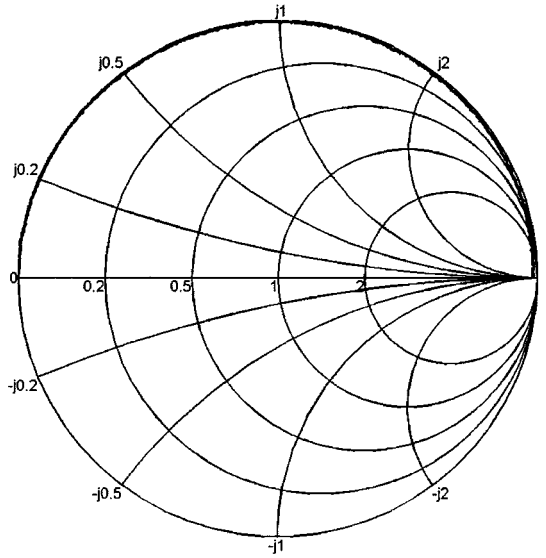


Fig. 7. Return loss of the line-extended *short* standard measured after calibration.

with better than −59 dB being typical across the 3-GHz band. The return loss after calibration varies by less than 2 dB over the entire band *at these small levels*, validating our assumption that the lumped element *load* standard maintains 75-Ω characteristic impedance of the transmission medium. In Fig. 7, we show the return loss of the *short* standard, extended by a CPW line with a round-trip delay of exactly a quarter-wavelength at 3 GHz, measured after calibration. Without the extension, the calibrated trace collapses about the extremity (−1, 0) in the reflection coefficient plane. The return loss of the extended *short* produces half a circumnavigation around the Smith chart, corresponding to a quarter-wavelength rotation. As expected, the increasing loss at the higher frequencies tends to rotate the trace inward. A similar agreement with the calibrated result is also observed for the line-extended *load* standard.

To summarize, the component measurement follows two steps.

Step 1) We perform a full two-port error correction using the *board calibration standards* shown in Fig. 4.

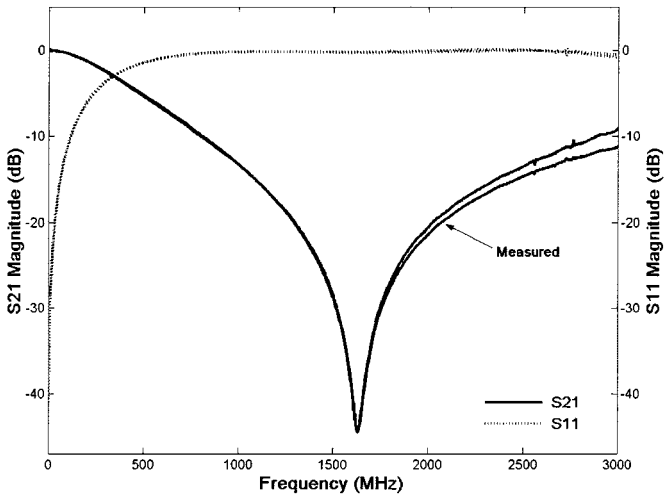
Step 2) We solder the SMD component over the pads depicted in Fig. 1, connect the NA cables to the fixture, and measure all four of the S-parameters.

The extraction of the component's equivalent circuit follows from the steps outlined in Section II. Sample measured results will be presented below.

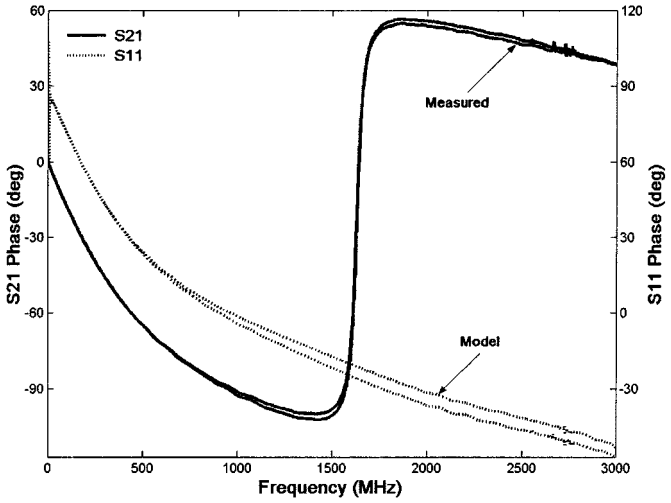
IV. Measured Results

A. Inductor Measured Data

The first example pertains to the measured data for a Coilcraft 68-nH ceramic inductor, mounted on an IEC 1206 SMD pad footprint. Fig. 8 displays the magnitude and phase of $S21$, as well as those of $S11$. The dip in transmission corresponds to parallel resonance between the inductor packaging and pad layout. In order to determine the resonant frequency and Q accurately, we calculate the impedance $Z(\omega)$ from the measured S-parameters, and plot its magnitude and phase in Fig. 9. The resonant



(a)



(b)

Fig. 8. (a) Magnitude and (b) phase of the measured S-parameters for a 68-nH SMD inductor.

frequency and Q at resonance are calculated from the magnitude curve as 1.682 GHz and 56.5, respectively. The peak resistance (at ω_0) is approximately 24 kΩ. It is clear that the reactance is predominantly inductive below the resonant frequency and capacitive above that frequency.

For comparison, we have also measured the same component using the HP 4291 impedance analyzer with the HP 16191 SMD test fixture. This instrument measures only the intrinsic characteristics of the component; hence, it does not capture the interaction between board layout and component package. The NA measurement does include the layout and package parasitic effects. The resonant frequency and quality factor for the impedance analyzer measurement are found to be 1.553 GHz and 30, respectively. It is evident that any equivalent-circuit CAD model derived from the impedance analyzer measurements will produce significant error in the design. Thus, it is very important to include package and layout parasitic effects in the CAD model. Incidentally, because the extrinsic model accounts for parasitic loading, our measured Q compares very well with the high-frequency Q of 55 reported in *Coilcraft's*

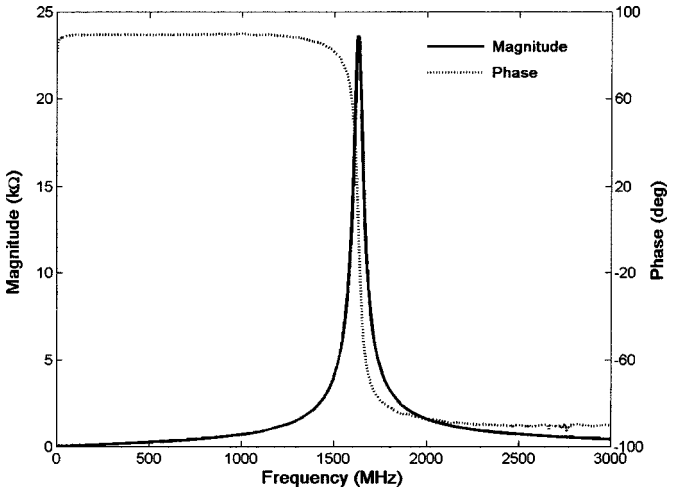


Fig. 9. Magnitude and phase of the impedance derived from measured data for a 68-nH SMD inductor.

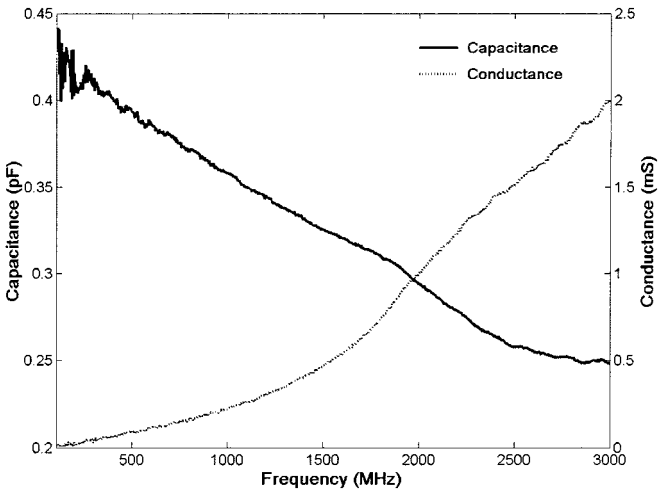


Fig. 11. Shunt conductance and capacitance of 1206-size pads measured with the 68-nH SMD.

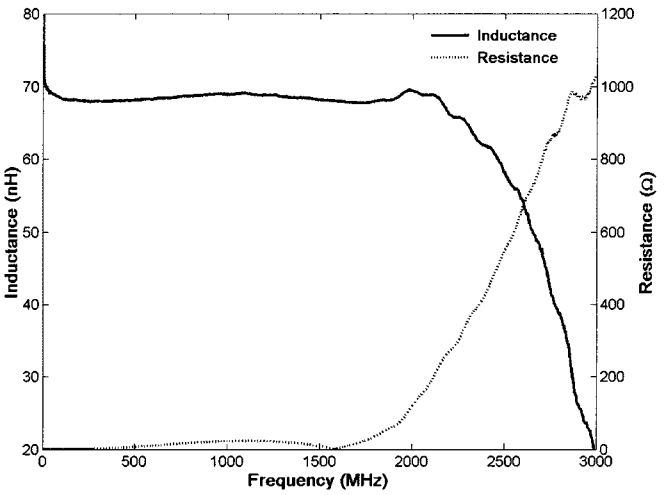


Fig. 10. Equivalent inductance and resistance of the 68-nH SMD package.

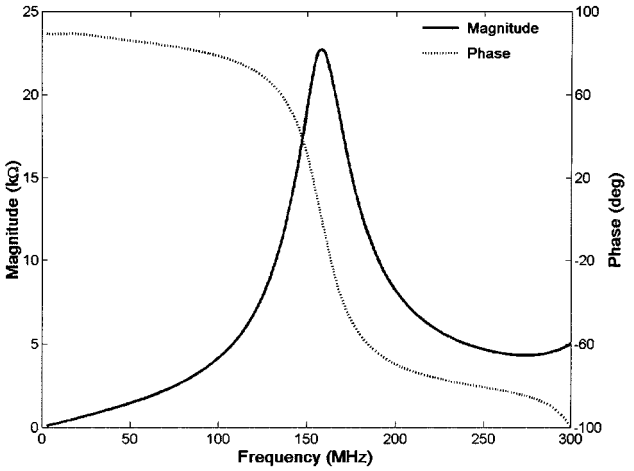


Fig. 12. Measured impedance (magnitude and phase) of the 13-turn RF choke.

March 1998 Catalog. Coilcraft uses a proprietary microstrip fixture with the NA to measure Q and f_0 of their inductors.

The inductance and resistance of the SMD package are shown in Fig. 10. The inductance lies between 68–70 nH up to the resonant frequency, where it dips abruptly and changes to a capacitance of 0.14 pF [calculated using (16)]. The resistance varies from 0.25 Ω to approximately 1 kΩ over the 3-GHz band, with a value of 5.3 Ω at resonance. Fig. 11 displays the shunt conductance and capacitance for the pads, calculated from (9) and (10), respectively. The conductance G_p is negligible (<2 mS over most of the band), indicating that dielectric loss is not a factor. The pad capacitance C_p remains between 0.25–0.42 pF over the 3-GHz bandwidth.

For comparison, we have overlaid in Fig. 8 the S-parameters computed using the frequency-dependent model depicted in Figs. 10 and 11. Excellent corroboration with measured result is observed for both magnitude and phase, especially near resonance.

Next, we have measured the S-parameters of a 13-turn RF choke wound on a ferrite core of relative permeability $\mu_r = 200$. The choke is intended to suppress RF interference around 150 MHz, and is thus a narrow-band device. The length of the winding is approximately equal to the gap between the component pads shown in Fig. 1, because of which the leads had to be bent inward and soldered on to the pads. Since the losses in the choke are quite high (low Q), this example presents a rigorous test case of the equivalent-circuit model developed in this research. Also, the strong magnetic leakage flux created by the ferrite core couples to the layout and influences the values of the pad parasitics manifested through the shunt admittance in Fig. 2. The computed series impedance near resonance is plotted in magnitude and phase in Fig. 12, and indicates $f_0 = 156.6$ MHz, $Q = 5.7$. The peak impedance at resonance is found to be 23.64 kΩ. The phase is around $\pm 90^\circ$ for significantly detuned frequencies, but changes by more than 30° as the frequency approaches resonance because of appreciable losses in the choke. In contrast, the SMD component (Fig. 9) maintains fairly constant detuned phase of $\pm 90^\circ$. The series inductance and resistance are plotted in Fig. 13. We observe that the inductance up to approximately 200 MHz compares very well with the nominal value of 4 μH. Due to increased power dissipation in the ferrite core and in the relatively large coil winding, the equivalent series resistance in Fig. 13 is quite high (approximately 1.1-kΩ

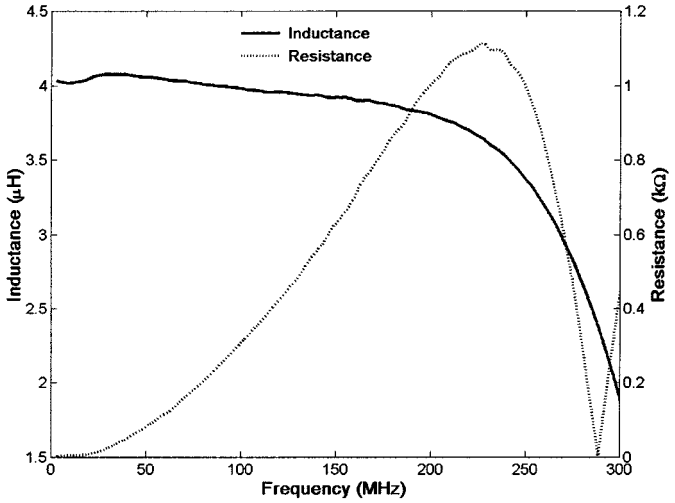


Fig. 13. Equivalent inductance and resistance of the 13-turn RF choke.

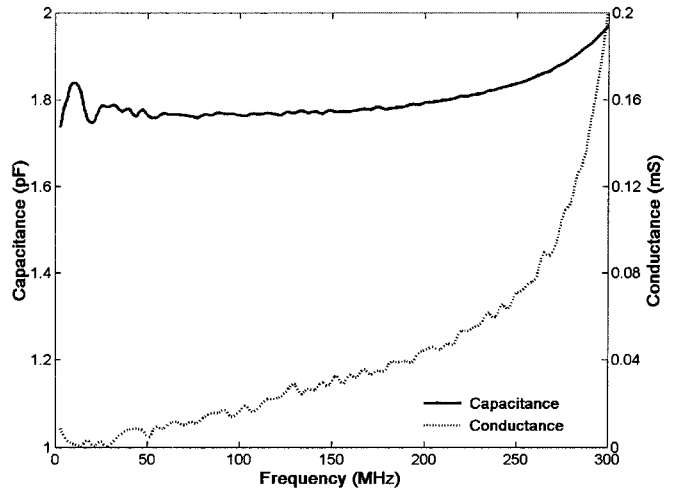
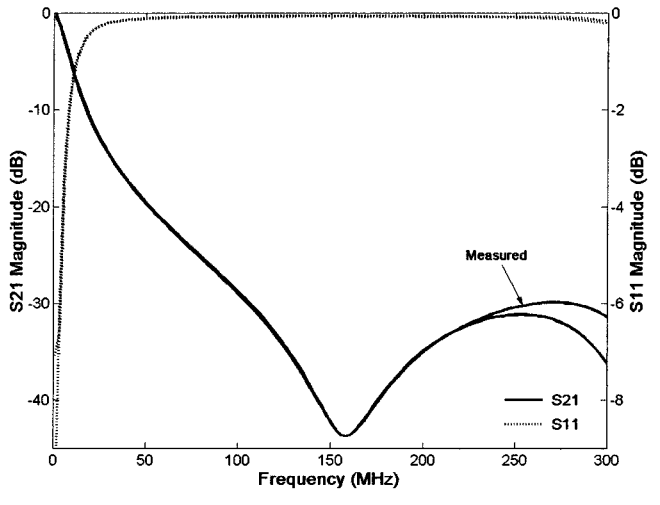
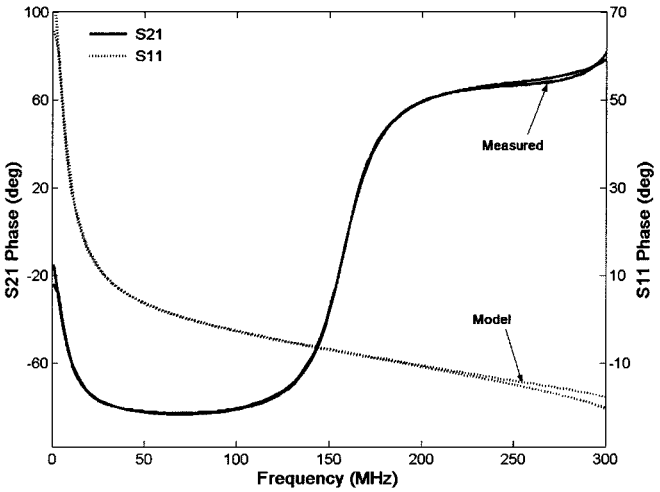


Fig. 14. Shunt conductance and capacitance of 1206-size pads measured with the RF choke.



(a)



(b)

Fig. 15. (a) Magnitude and (b) phase of the measured S-parameters for the RF choke. For comparison, data derived from the model are also displayed.

peak). The resistance at resonance is approximately 600 Ω for the choke in contrast to 5 Ω for the SMD inductor. The self-capacitance of the ferrite choke, including the core and winding capacitances, yields $C = 0.28$ pF in the model. The shunt capacitance for the pads, depicted in Fig. 14, is approximately 1.8–2 pF over a 300-MHz bandwidth, a factor of 6–10 times larger than the value associated with ceramic SMD inductors. The increase in shunt capacitance can be partially attributed to self-capacitance (to ground) of the ferrite core, which has a relatively high dielectric constant (approximately 16). The proximity coupling between the winding and pads also contributes to this increase. However, the shunt conductance of the pads is still small, indicating that the dielectric loss can be neglected. This example emphasizes the importance of characterizing interaction between the component and layout through extrinsic modeling. In order to validate the equivalent-circuit model, we computed Z and Y_p in (1) and (2) using the derived values of $R(\omega)$, $L(\omega)$, $G_p(\omega)$, $C_p(\omega)$, and C (as plotted in Figs. 13 and 14), calculated the corresponding S-parameters of the choke model, and compared them with the measured data for the choke. Fig. 15 reveals an excellent agreement between model and measurement in both magnitude and phase of the S-parameters. This close agreement between model and measurement is gratifying given that the RF choke is a difficult test case, manifesting strong coupling and increased loss around resonance. A circuit validation of the inductor model will be presented at the conclusion of this section.

B. Capacitor Measured Data

Fig. 16 displays the measured admittance magnitude and phase of a shunt-connected 1.5-pF SMD capacitor from AVX, attached between ground and a 75-Ω CPWG transmission line. The S-parameters were measured using a 6-GHz 8753 NA with a 50–75-Ω coaxial transformer. The measured frequency at antiresonance is given by $f_0 = 5.107$ GHz, and $Q = 53.2$, with minimum impedance at antiresonance of 0.402 Ω. The phase of the admittance $-Y(1,2)$, obtained by adding 180° to the data in Fig. 16, is clearly 90° for frequencies lower than the resonance, and changes to −90° after the resonance. The inductance of the capacitor package, determined from (15), is found to be $L_0 = 0.67$ nH, which is a small value. The model's frequency-dependent capacitance and resistance are plotted in Fig. 17. The capacitance is approximately 1.5 pF at 50 MHz,

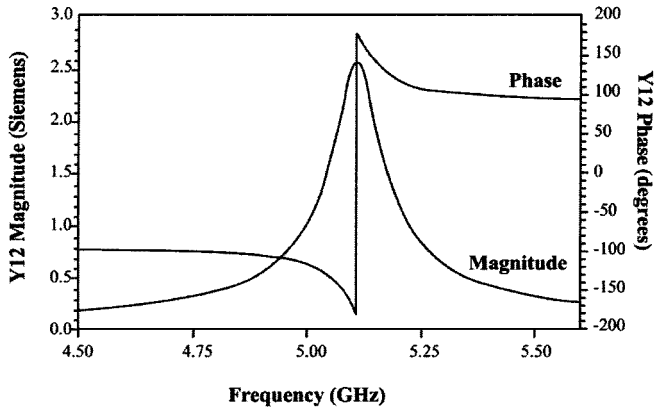


Fig. 16. Measured admittance of a 1.5-pF SMD capacitor in 0805 package style.

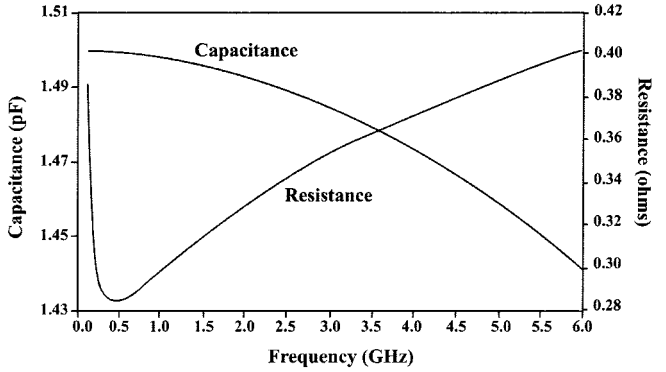


Fig. 17. Equivalent-circuit parameters of the 1.5-pF SMD capacitor.

and decreases to 1.44 pF at 6 GHz. The resistance over the 6-GHz band is below 0.5 Ω. Although not shown for brevity, the S-parameters of the model compared very well with the measurements over the entire band. Further validation of the shunt-capacitor model will be given in the filter design example to follow.

C. Interconnect Characterization

We have measured the S-parameters of a CPWG line using the same measurement fixture as the components. The line has a nominal characteristic impedance of 75 Ω. Various lengths of this line are used to interconnect components in a low-pass filter that we will present in the following section. Using the measured data on the line, we have computed the characteristic impedance and propagation constant of the interconnect as follows:

$$Z_c = \sqrt{Z_{11}^2 - Z_{12}^2} \tag{24}$$

$$\gamma\ell = \cosh^{-1}\left(\frac{Z_{11}}{Z_{22}}\right) = \log\left(\frac{Z_{11}}{Z_{22}} + \sqrt{\left(\frac{Z_{11}}{Z_{22}}\right)^2 - 1}\right) \tag{25}$$

where ℓ is the length of the interconnect. The open-circuit impedance (Z) parameters in (24) and (25) are obtained by transforming the measured S-parameters. The attenuation and phase constant of the line are calculated from the real and imaginary parts in (25).

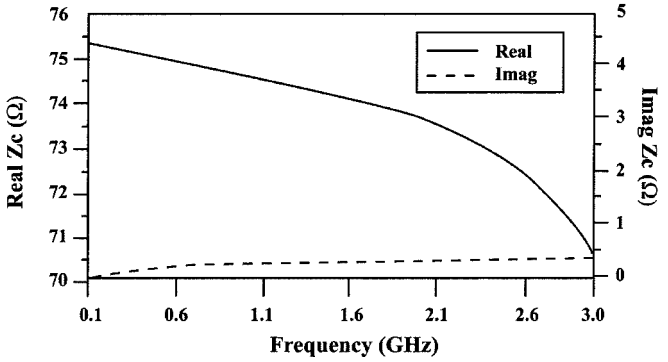


Fig. 18. Characteristic impedance of the CPWG interconnect.

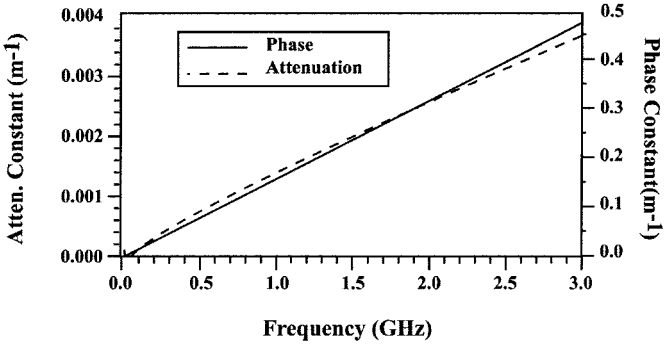


Fig. 19. Attenuation and phase constants of the CPWG interconnect.

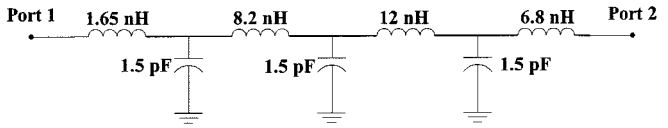


Fig. 20. Schematic of the ideal lumped-element-prototype of a Chebyshev low-pass filter.

Fig. 18 depicts the characteristic impedance of the CPWG interconnect, which is close to 75 Ω at low frequencies, and drops to approximately 70.5 Ω at 3 GHz. The imaginary part of Z_c stays below 0.4 Ω across the band. The attenuation and phase constants are plotted in Fig. 19. The transmission line shows a small attenuation and fairly linear phase shift with frequency. The line parameters calculated from the measured data are used to model all the interconnects used in the validation design to follow.

D. Circuit Validation

We have designed a low-pass filter in a CPWG transmission medium to validate the measured inductor and capacitor models presented in this paper. The *ideal prototype* fifth-order Chebyshev response has a ripple of 0.2 dB in the passband, cutoff frequency of 1 GHz, and a minimum stopband attenuation of 30 dB at 2 GHz. The schematic of the ideal filter prototype is shown in Fig. 20, and the associated layout implementation is shown in Fig. 21 with the SMD components connected by approximately 0.2-in-long CPW transmission lines. The SMD elements have been first measured in the CPWG fixture, and their *extrinsic* equivalent-circuit models characterized as discussed in Section II. Next, using these measured models and the interconnect's transmission-line parameters computed in Section IV-C, we have calculated the S-parameters of the circuit in Fig. 21.

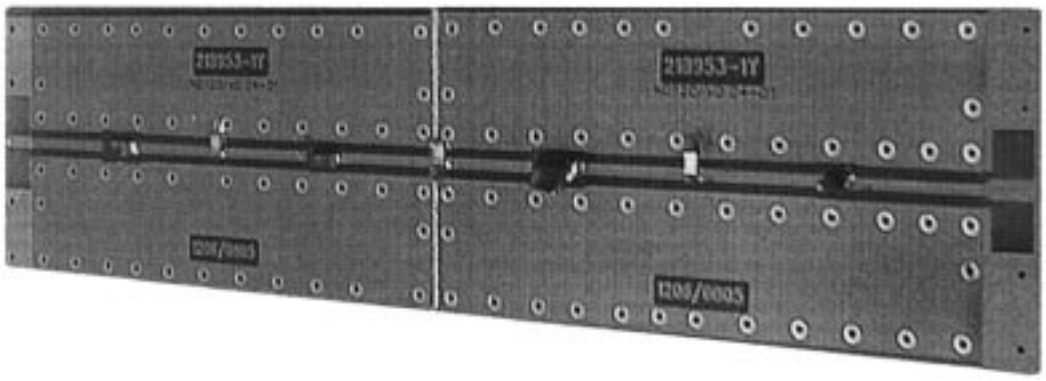


Fig. 21. Layout implementation of the low-pass filter showing the SMD component locations and CPW interconnects.

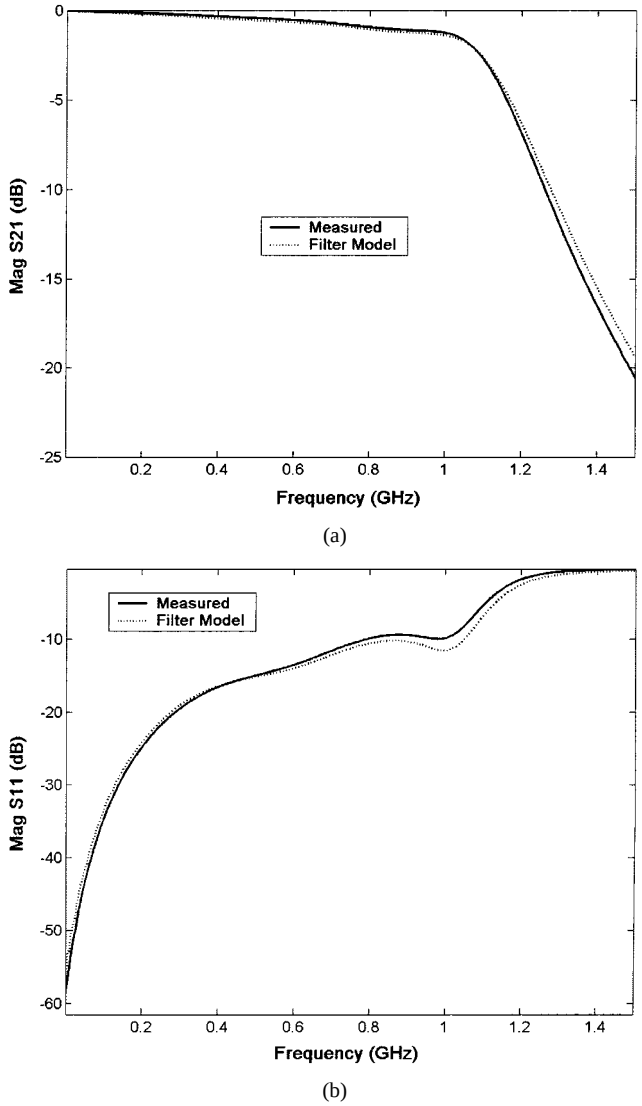


Fig. 22. Correlation between the filter's measured S-parameters and circuit model. (a) Insertion loss. (b) Return loss.

It is emphasized that no layout simulations (such as the moment method) were used to calculate the circuit response. The entire response, termed as the *filter model* in the ensuing discussion, is obtained by using standard circuit theory and the *extrinsic* discrete component models. All the layout parasitic effects and other interactions with components are resident in the latter equivalent-circuit models. The resulting S-parameter magnitude response of the *filter model* is plotted in Fig. 22. The insertion loss within the passband is observed to be less than 1.5 dB, and the cutoff characteristics are within the specifications. The return loss is lower than 10 dB over the passband. *An interesting feature of the design is that, by incorporating measured models for interconnects and the discrete components, the circuit did not require any tuning to meet the specifications*. For comparison, the measured insertion and return losses of the CPW filter are also plotted in Fig. 22. The agreement between the filter model and measured data is within 0.2 dB in the passband, and the worst-case discrepancy in $S11$ is approximately 2 dB (but the reflected signal is below a 10-dB level). The phase of $S11$ and $S21$ also showed reasonable correlation between the filter model and measurement, but are not plotted for brevity.

V. Conclusions

We have presented a method to derive extrinsic equivalent-circuit models of RF components, which consider the parasitic effects of the design environment such as layout and package effects, material loss, etc. The model is derived in *closed form* from S-parameters measured on an NA without using any numerical optimization normally followed in RF circuit synthesis. We have demonstrated the procedure for SMD inductors and capacitors, focusing on the advantages of extrinsic over intrinsic modeling. We have validated the derived *extrinsic* component models by incorporating them in a low-pass CPW filter design, and demonstrated good correlation between the model and measurement in the filter response. We have shown that the increased accuracy, attained by incorporating layout/package parasitic effects of the SMD devices and measured transmission-line parameters of the interconnects, allows for easier design centering, as evidenced by first-pass design success on the filter.

Appendix

We now derive the inductor and capacitor model parameters in (17), (18), and (23). To derive the inductance $L(\omega)$ in (17), we start with the admittance, given by the reciprocal of $Z(\omega)$ in (1)

$$Y \triangleq Y_r + jY_i = \frac{R}{R^2+\omega^2L^2} + j\omega\left(C_0 - \frac{L}{R^2+\omega^2L^2}\right). \quad (26)$$

It is emphasized that R and L are functions of frequency; the subscript on C in (26) simply indicates that the capacitance C_0 is constant with frequency [see (16)]. R can be expressed in terms of L using the real part in (26)

$$R = \frac{1 \pm \sqrt{1-(2Y_r\omega L)^2}}{2Y_r}. \tag{27}$$

The imaginary part in (26) may be written as

$$Y_i = \omega C_0 - \frac{\omega L Y_r}{R}. \tag{28}$$

Substituting for R from (27) in (28) yields a quadratic equation for L of the form

$$X \pm \sqrt{X^2-1} = \frac{Y_r}{\omega C_0 - Y_i} \triangleq A, \qquad \text{with } X \triangleq \frac{1}{2\omega L Y_r}. \tag{29}$$

Solving (29) for X in terms of A, we obtain

$$X = \frac{1+A^2}{2A}. \tag{30}$$

Back-substituting for X and A from (29) results in the sought-after expression for $L(\omega)$ as follows:

$$L(\omega) = \frac{1}{\omega\left[\omega C_0 + \dfrac{|Y|^2 - \omega C_0 Y_i}{\omega C_0 - Y_i}\right]}. \tag{31}$$

Realizing that $|Y| = 1/|Z|$, $Y_r = Z_r/|Z|^2$ and $Y_i = -|Z_i/|Z|^2|$, after simplification, (31) yields (17).

Substitution of ωL from (31) into (28) results in the expression for the resistance

$$R(\omega) = \frac{Y_r}{(\omega C_0)^2 - 2\omega C_0 Y_i + |Y|^2}. \tag{32}$$

By writing Y_r, Y_i, and $|Y|$ in terms of Z_r, Z_i, and $|Z|$, we then obtain $R(\omega)$ in (18).

To derive (23) for the capacitance $C(\omega)$, we observe that the imaginary part of (20) may be written as

$$\left(\frac{\omega_0}{\omega}\right)^2 \frac{C_0}{C(\omega)} = 1 - \frac{Z_i(\omega)\omega_0}{\omega Q R_0}. \tag{33}$$

Solving for C, we obtain (23) after elimination of Q and ω_0 using (12) and (19), respectively.

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